

CLAIMS

What is claimed is:

- 1 1. A switching topology for automatic test equipment, comprising:
2 a plurality of switching circuits each having first through fourth nodes, wherein
3 the first and second nodes are connectable to the third and fourth nodes, respectively, to
4 form a THROUGH connection, or to the fourth and third nodes, respectively, to form a
5 CROSSED connection,
6 wherein each of the first through fourth nodes of any of the plurality of switching
7 circuits is connected to at most one of the first through fourth nodes of all the others of
8 the plurality of switching circuits.
- 1 2. A switching topology as recited in claim 1, wherein each of the plurality of
2 switching circuits comprises first and second switching elements each having a common
3 point and first and second connection points to which the common point is selectively
4 connectable.
- 1 3. A switching topology as recited in claim 2, wherein, for each of the plurality of
2 switching circuits,
3 the first and second nodes are the common points of the first and second
4 switching elements, respectively,
5 one of the first and second connection points of the first switching element is
6 connected to one of the first and second connection points of the second switching
7 element to form the third node of the switching circuit,
8 the other of the first and second connection points of the first switching element is
9 connected to the other of the first and second connection points of the second switching
10 element to form the fourth node of the switching circuit.
- 1 4. A switching topology as recited in claim 3, wherein the first and second switching
2 elements are form-C relays.
- 1 5. A switching topology as recited in claim 4, wherein the form-C relays for the first
2 and second switching elements are located together in a dual form-C package.

- 1 6. A switching topology as recited in claim 5, wherein all connections between the
2 first and second switching elements are formed within the dual form-C package.
- 1 7. A switching topology as recited in claim 5, wherein the first and second switching
2 elements are controlled together in response to a single control signal.
- 1 8. A switching topology as recited in claim 1, wherein the switching circuits are
2 implemented with micro-machined switches.
- 1 9. A switching topology as recited in claim 1, wherein the switching circuits are
2 implemented with solid-state switches.
- 1 10. A switching topology as recited in claim 1, wherein the plurality of switching
2 circuits is arranged in the form of at least first through fourth N-by-N switching units
3 each comprising at least one of the plurality of switching circuits,
4 wherein N/2 nodes of the first N-by-N switching unit is coupled to N/2 nodes of
5 the third N-by-N switching unit,
6 wherein N/2 nodes of the second N-by-N switching unit is coupled to N/2 nodes
7 of the fourth N-by-N switching unit,
8 wherein N/2 nodes of the first N-by-N switching unit is coupled to N/2 nodes of
9 the fourth N-by-N switching unit, and
10 wherein N/2 nodes of the second N-by-N switching unit is coupled to N/2 nodes
11 of the third N-by-N switching unit.
- 1 11. A switching topology as recited in claim 10, further comprising a fifth N-by-N
2 switching unit having N/2 nodes coupled to each of the first through fourth N-by-N
3 switching units.
- 1 12. A switching topology as recited in claim 10, further comprising an additional pair
2 of N-by-N switching units, each of said additional pair of N-by-N switching units having
3 N/2 nodes coupled to each of the third and fourth N-by-N switching units.
- 1 13. A switching topology as recited in claim 10, wherein N is a power of 2.
- 1 14. A switching topology as recited in claim 10, wherein N equals 2, and further
2 comprising:

3 a fifth N-by-N switching unit having $N/2$ nodes coupled to each of the first
4 through fourth N-by-N switching units.

1 15. A switching topology as recited in claim 10, wherein N equals 2, and further
2 comprising:
3 an additional pair of N-by-N switching units, each of said additional pair of N-by-
4 N switching units having $N/2$ nodes coupled to each of the third and fourth N-by-N
5 switching units.

1 16. A method of switching signals in an automatic test system, comprising:
2 providing an array of switching circuits each having a first pair of nodes and a
3 second pair of nodes; and
4 for each switching circuit, alternatively passing or crossing signals applied to the
5 first pair of nodes for provision to the second pair of nodes,
6 wherein each node of any of the plurality of switching circuits is coupled to no
7 greater than one node of any other of the plurality of switching circuits.

1 17. A method as recited in claim 16, wherein the automatic test system includes tester
2 resources that are connectable, via the array of switching circuits, to nodes of a unit under
3 test for conducting tests on the unit under test.

1 18. A method as recited in claim 17, further comprising:
2 applying a first signal to the unit under test via the array of switching circuits;
3 receiving a second signal from the unit under test via the array of switching
4 circuits;
5 testing whether the second signal is within an allowable range prescribed for the
6 unit under test.

1 19. A method as recited in claim 18, further comprising:
2 determining a passing or failing test status of the unit under test responsive to
3 whether the second signal is within the allowable range or outside the allowable range.

1 20. An automatic test system, comprising:
2 a plurality of tester resources;
3 an interface for receiving a unit under test; and

4 a plurality of switching circuits coupled between the plurality of tester resources
5 and the interface for selectively coupling the tester resources to nodes of the unit under
6 test,
7 wherein each switching circuit has a first pair of nodes, a second pair of nodes,
8 and a control input,
9 wherein a pair of signals applied to the first pair of nodes of a switching circuit is
10 either passed or crossed enroute to the second pair of nodes responsive to a control signal
11 applied to the control input, and
12 wherein each node of any of the plurality of switching circuits is coupled to no
13 greater than one node of any other of the plurality of switching circuits.